数字电路与逻辑设计B

第二十讲

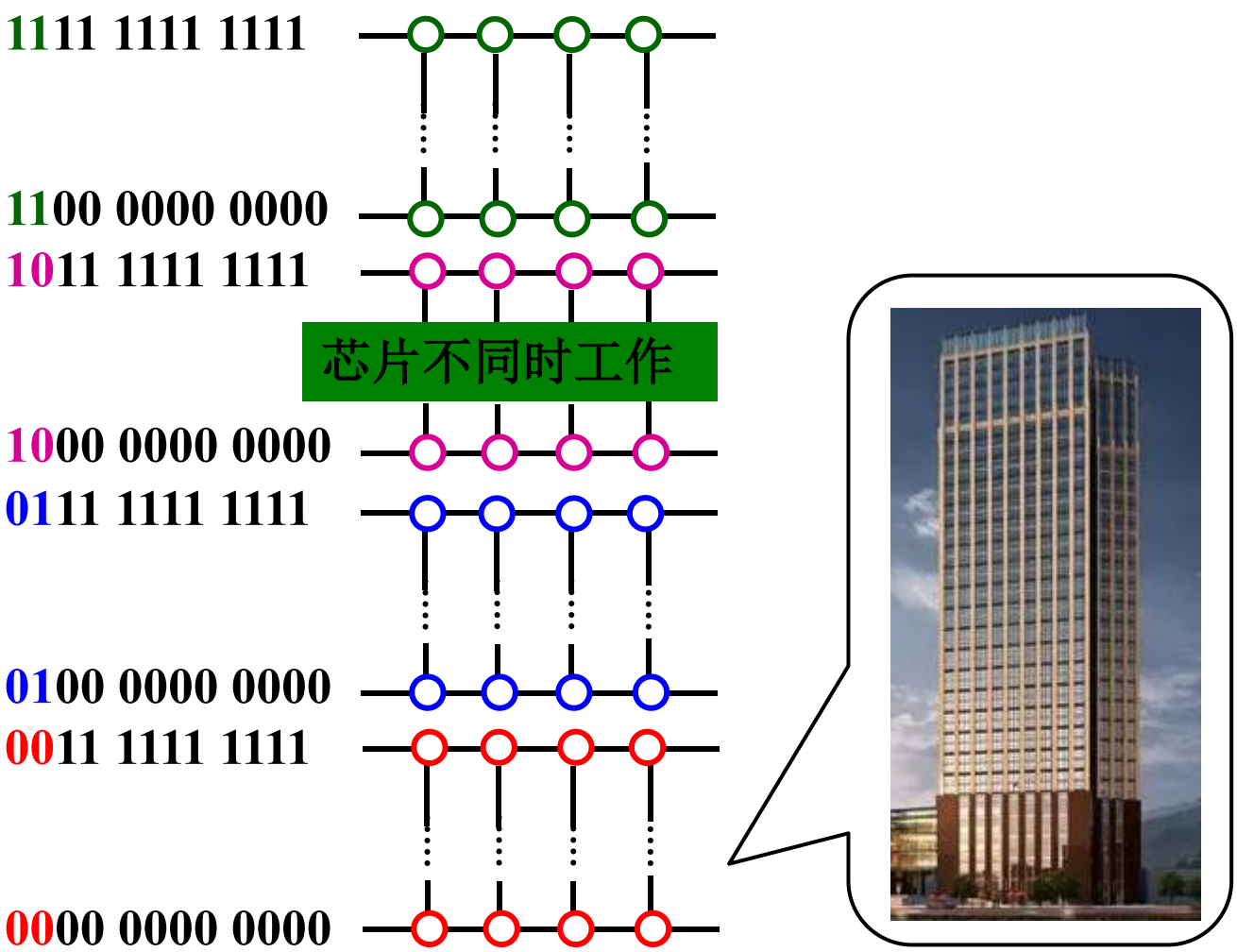
南京邮电大学

电子与光学工程学院

臧裕斌

3.存储容量的扩展

1)字扩展 1024 × 4 ⇒ 4096 × 4

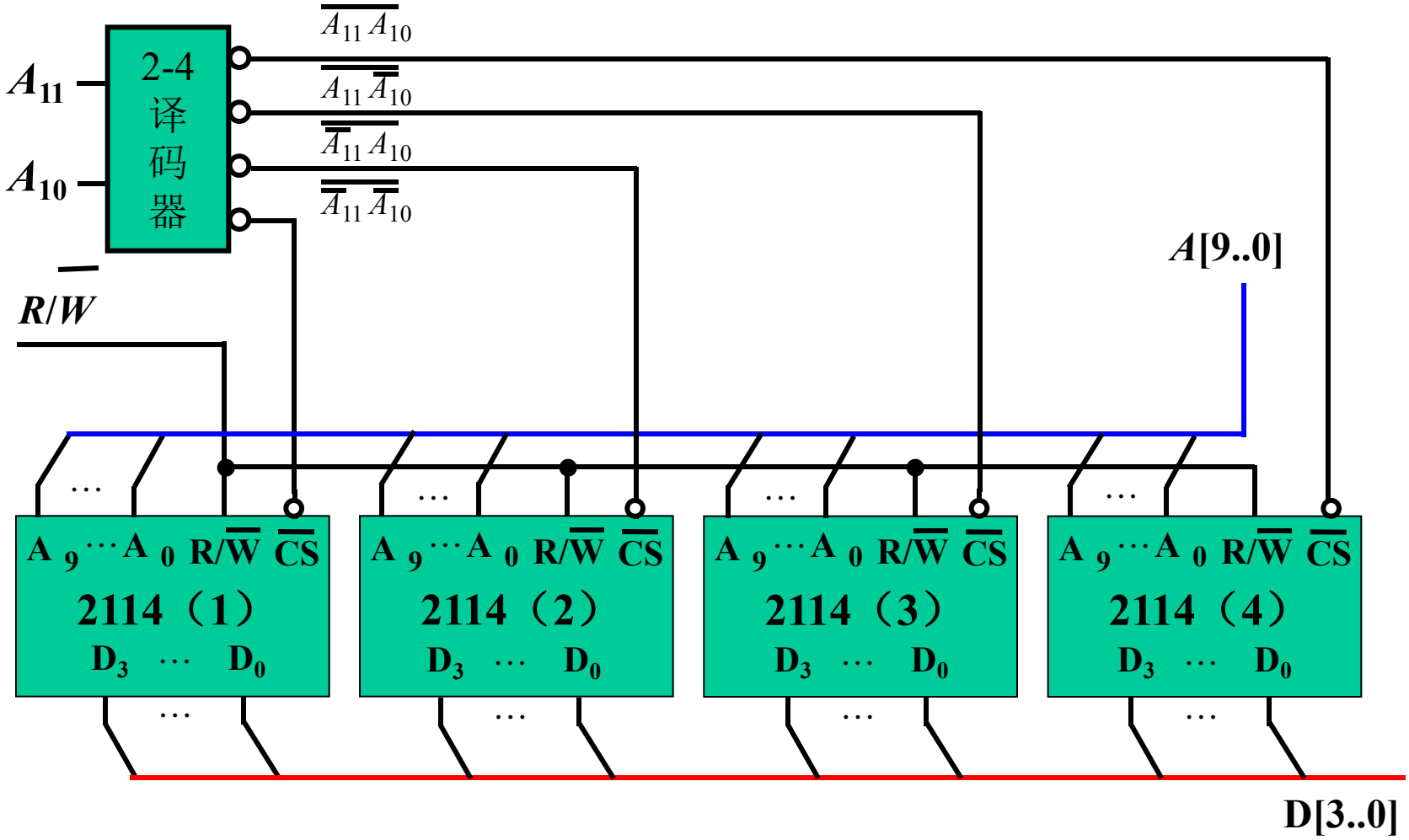


$A_{11}A_{10}$	选中片号	对应地址范围	
0 0	2114(1)	0～1023	00 0…0～00 1…1
0 1	2114(2)	1024～2047	01 0…0～01 1…1
1 0	2114(3)	2048～3071	10 0…0～10 1…1
1 1	2114(4)	3072～4095	11 0…0～11 1…1

$A_{11}A_{10}$	选中片号	$\overline{CS(1)}$	$\overline{CS(2)}$	$\overline{CS(3)}$	$\overline{CS(4)}$
0 0	2114(1)	0	1	1	1
0 1	2114(2)	1	0	1	1
1 0	2114(3)	1	1	0	1
1 1	2114(4)	1	1	1	0

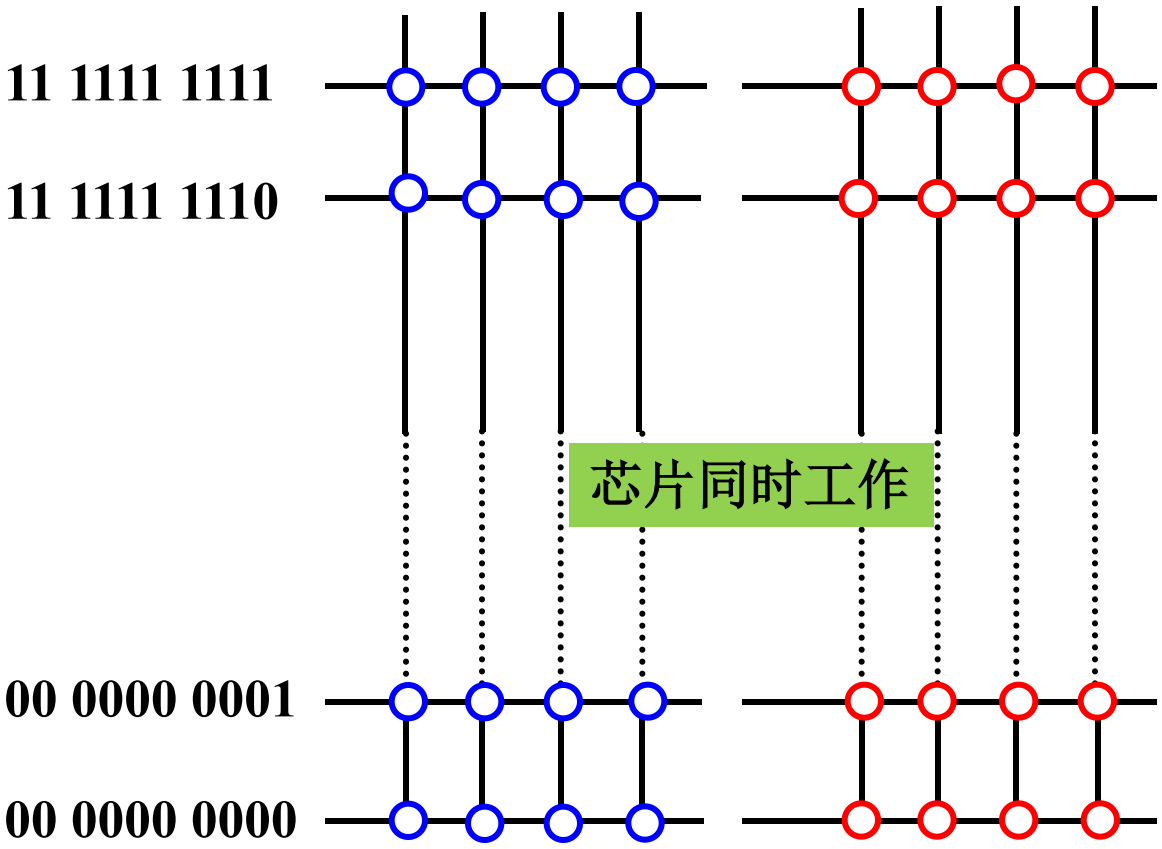
$$CS(1) = \overline{\overline{A}_{11}\overline{A}_{10}} \qquad CS(3) = \overline{A_{11}\overline{A}_{10}}$$

$$CS(2) = \overline{\overline{A}_{11}A_{10}} \qquad CS(4) = \overline{A_{11}A_{10}}$$

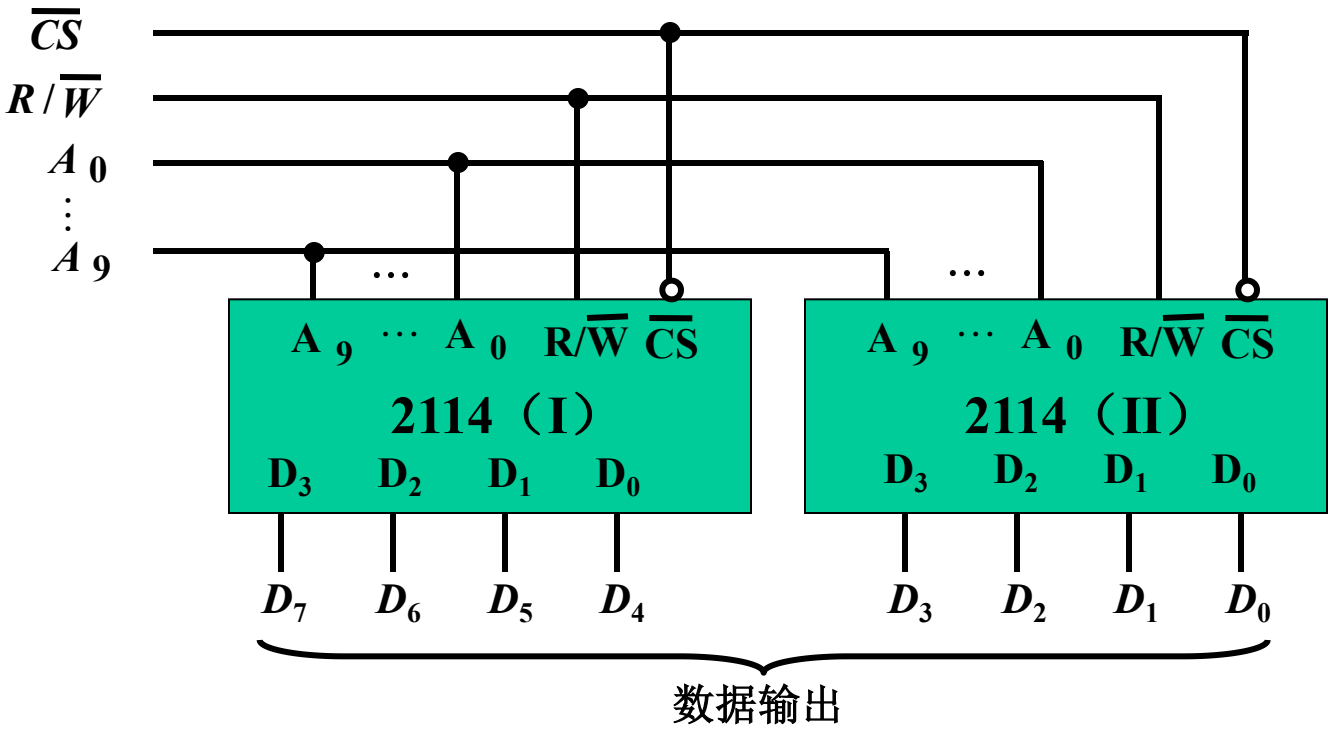

A_{11}
A_{10}
2-4
译
码
器
$\overline{A_{11}}\,\overline{A_{10}}$
$A_{11}\,\overline{A_{10}}$
$\overline{A_{11}}\,A_{10}$
$A_{11}\,A_{10}$
A[9..0]
$R/\overline{W}$
A 9 … A 0 R/W CS
2114（1）
D3 … D0
A 9 … A 0 R/W CS
2114（2）
D3 … D0
A 9 … A 0 R/W CS
2114（3）
D3 … D0
A 9 … A 0 R/W CS
2114（4）
D3 … D0
D[3..0]

2114芯片字扩展

2) 位扩展　1024 × 4 ⇒ 1024 × 8

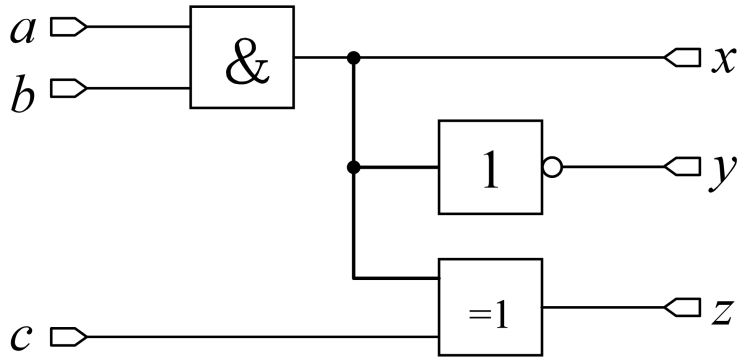


位扩展示意图


$\overline{CS}$
$R/\overline{W}$
A_0
A_9
A_9 … A_0 R/$\overline{W}$ $\overline{CS}$
2114（I）
D_3 D_2 D_1 D_0
A_9 … A_0 R/$\overline{W}$ $\overline{CS}$
2114（II）
D_3 D_2 D_1 D_0
D_7 D_6 D_5 D_4
D_3 D_2 D_1 D_0
数据输出

6.3 PLA&PAL

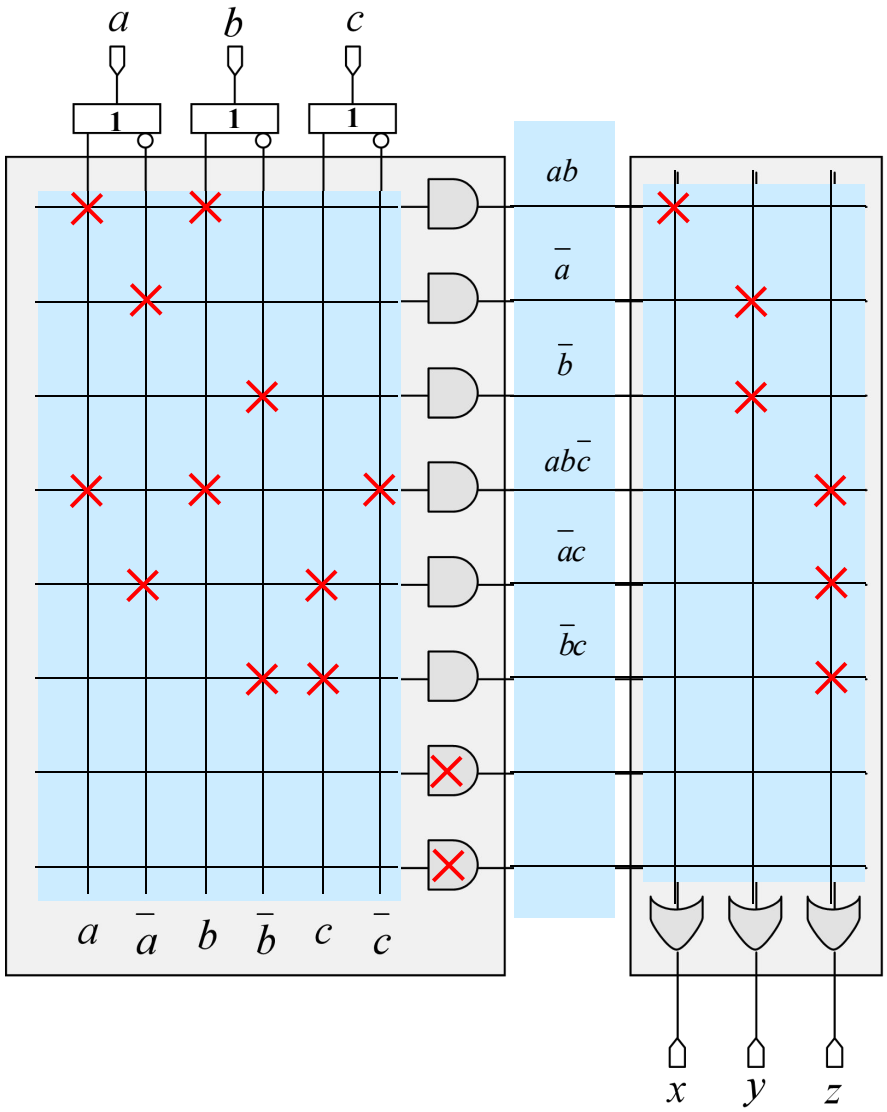
【例】用PLA实现如下电路。



$$x = ab$$

$$y = \overline{ab} = \bar{a} + \bar{b}$$

$$z = ab \oplus c = ab \cdot \bar{c} + \overline{ab} \cdot c = ab\bar{c} + \bar{a}c + \bar{b}c$$

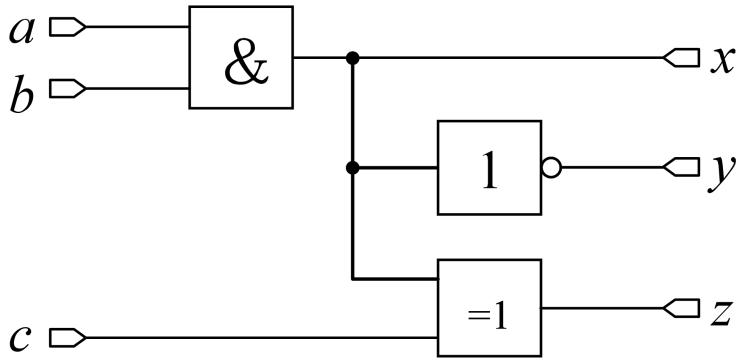


$$x = ab$$

$$y = \overline{ab} = \bar{a} + \bar{b}$$

$$z = ab\bar{c} + \bar{a}c + \bar{b}c$$

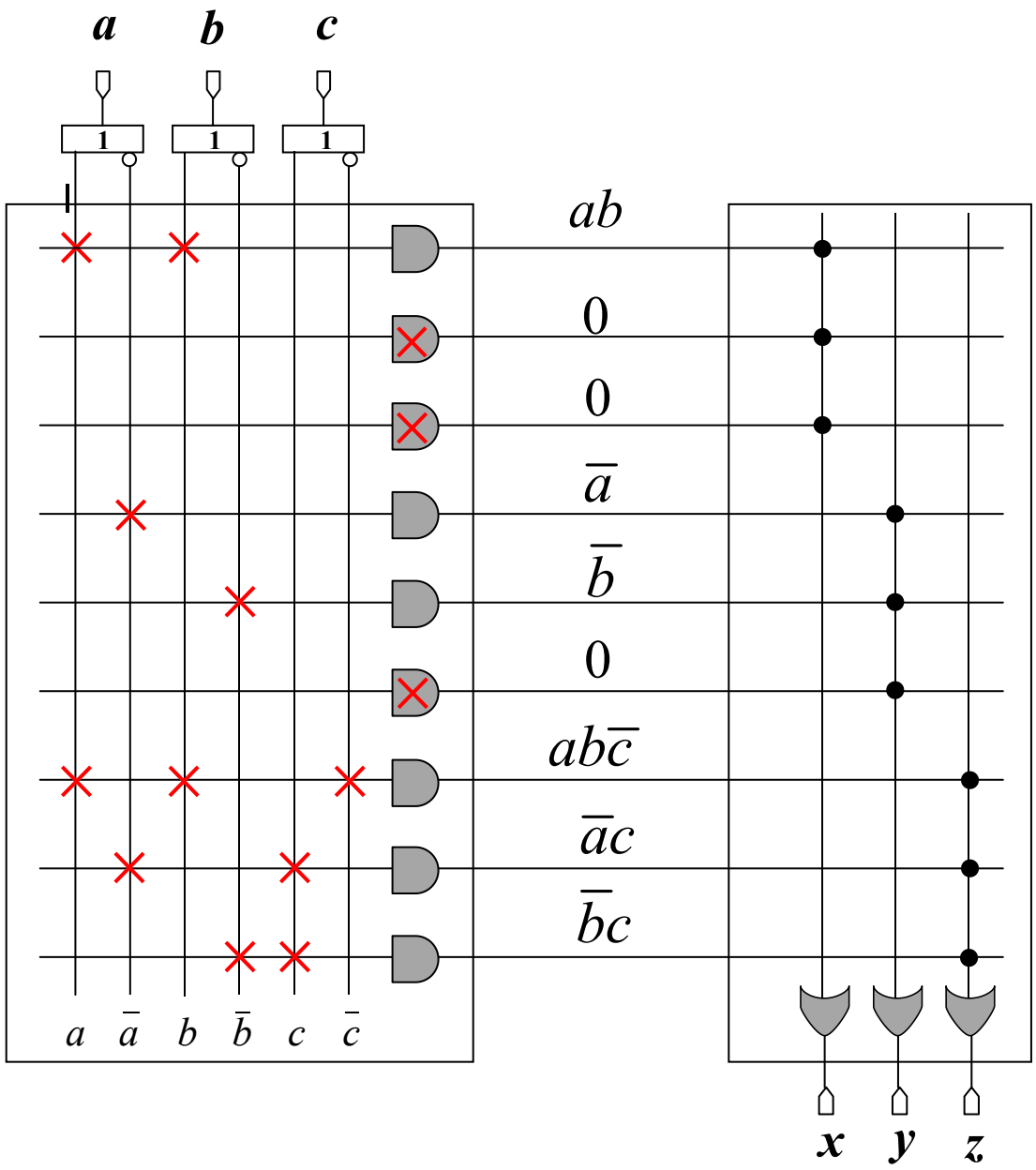
【例】用PAL实现如下电路。



$$x = ab$$

$$y = \overline{ab} = \bar{a} + \bar{b}$$

$$z = ab \oplus c = ab \cdot \bar{c} + \overline{ab} \cdot c = ab\bar{c} + \bar{a}c + \bar{b}c$$



$$x = ab$$

$$y = \overline{ab} = \bar{a} + \bar{b}$$

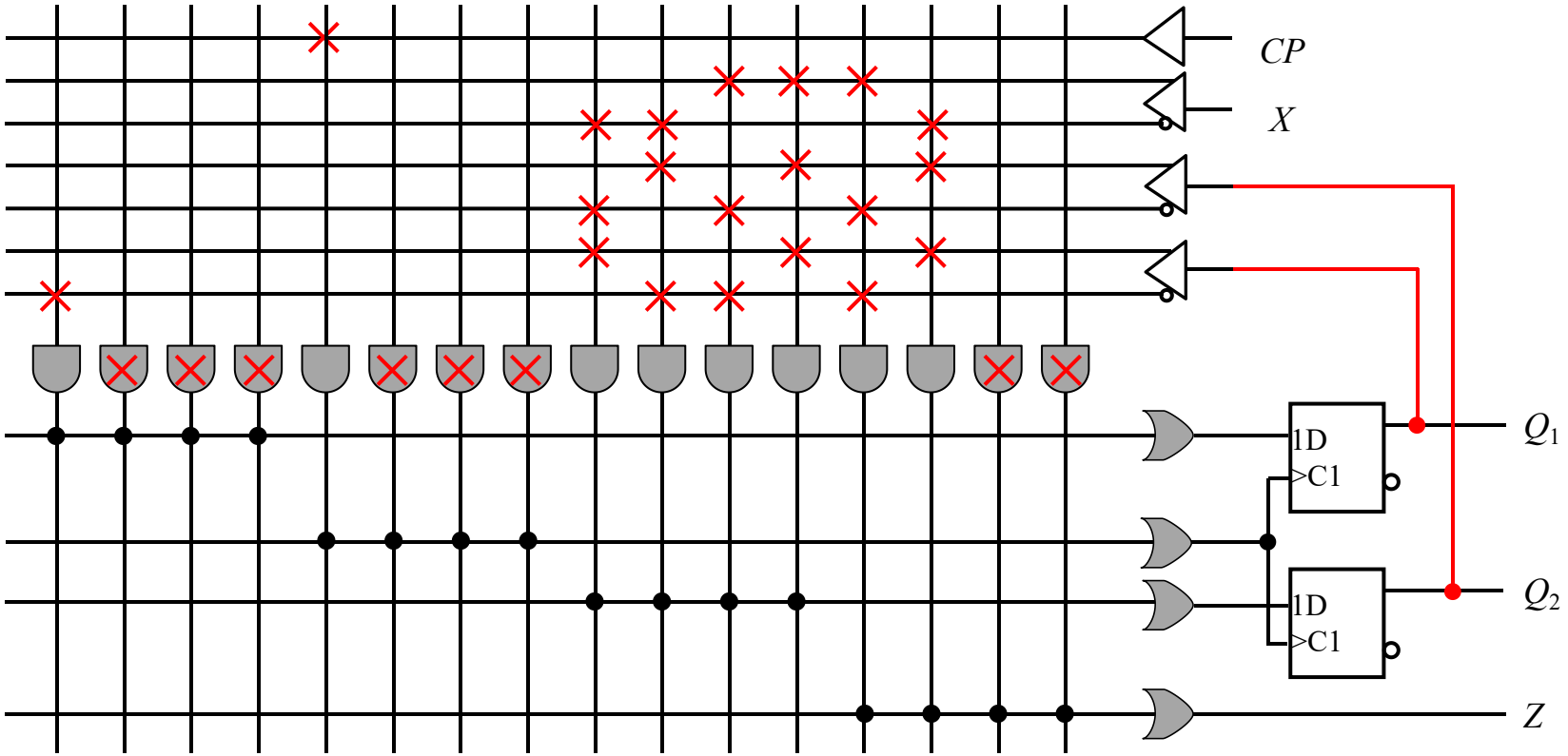
$$z = ab\bar{c} + \bar{a}c + \bar{b}c$$

【例】用PAL实现如下函数。

$$Q_2^{n+1} = \bar{X}Q_1^n\bar{Q}_2^n + \bar{X}\bar{Q}_1^nQ_2^n + X\bar{Q}_1^n\bar{Q}_2^n + XQ_1^nQ_2^n$$

$$Q_1^{n+1} = \bar{Q}_1^n$$

$$Z = X\bar{Q}_1^n\bar{Q}_2^n + \bar{X}Q_1^nQ_2^n$$

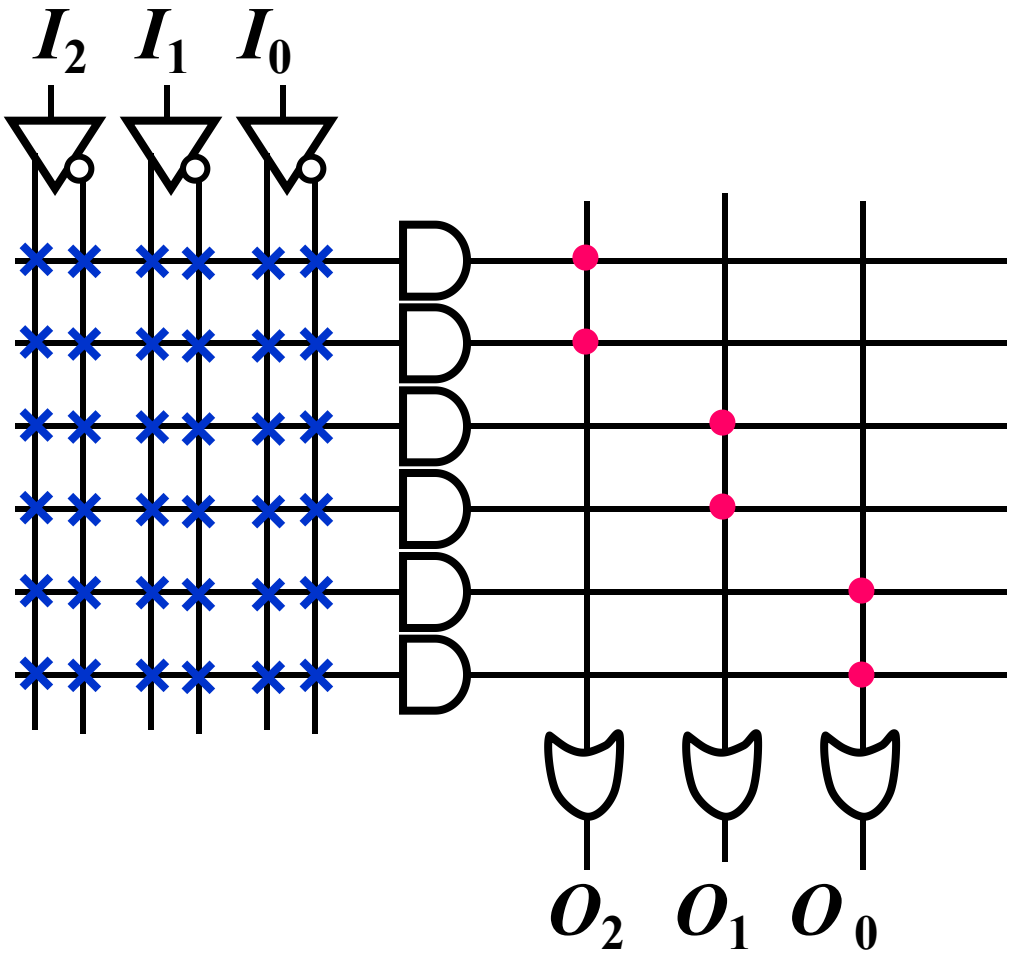


$$Q_2^{n+1} = \bar{X}Q_1^n\bar{Q}_2^n + \bar{X}\bar{Q}_1^nQ_2^n + X\bar{Q}_1^n\bar{Q}_2^n + XQ_1^nQ_2^n$$

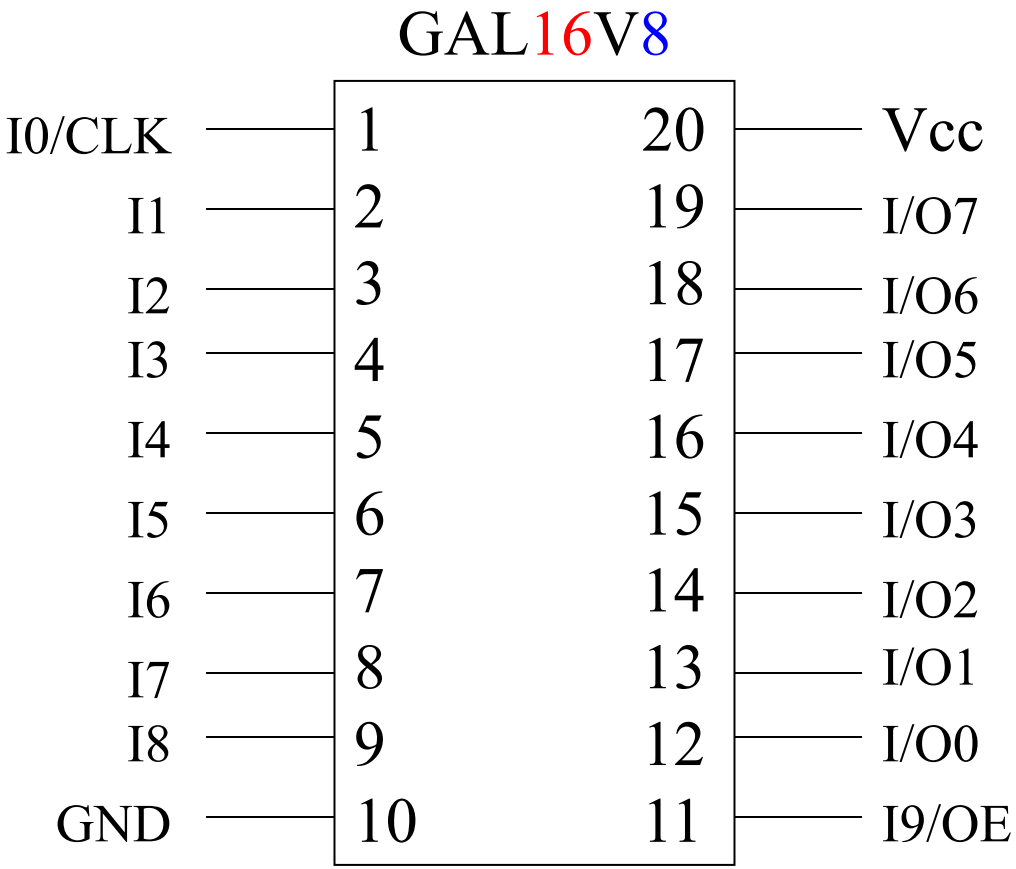
$$Q_1^{n+1} = \bar{Q}_1^n$$

$$Z = X\bar{Q}_1^n\bar{Q}_2^n + \bar{X}Q_1^nQ_2^n$$

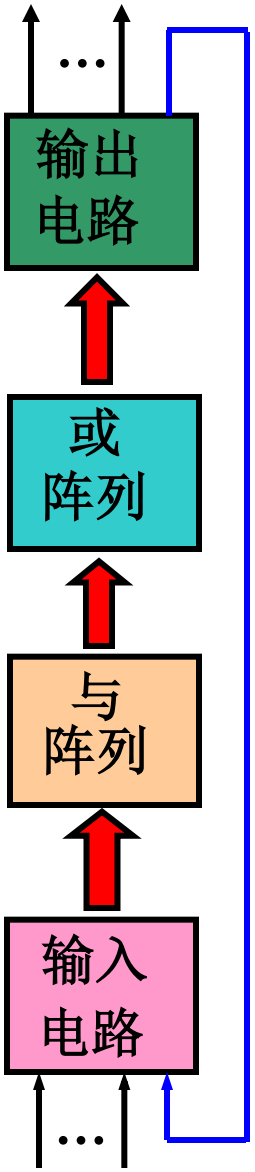
6.4 通用阵列逻辑 GAL

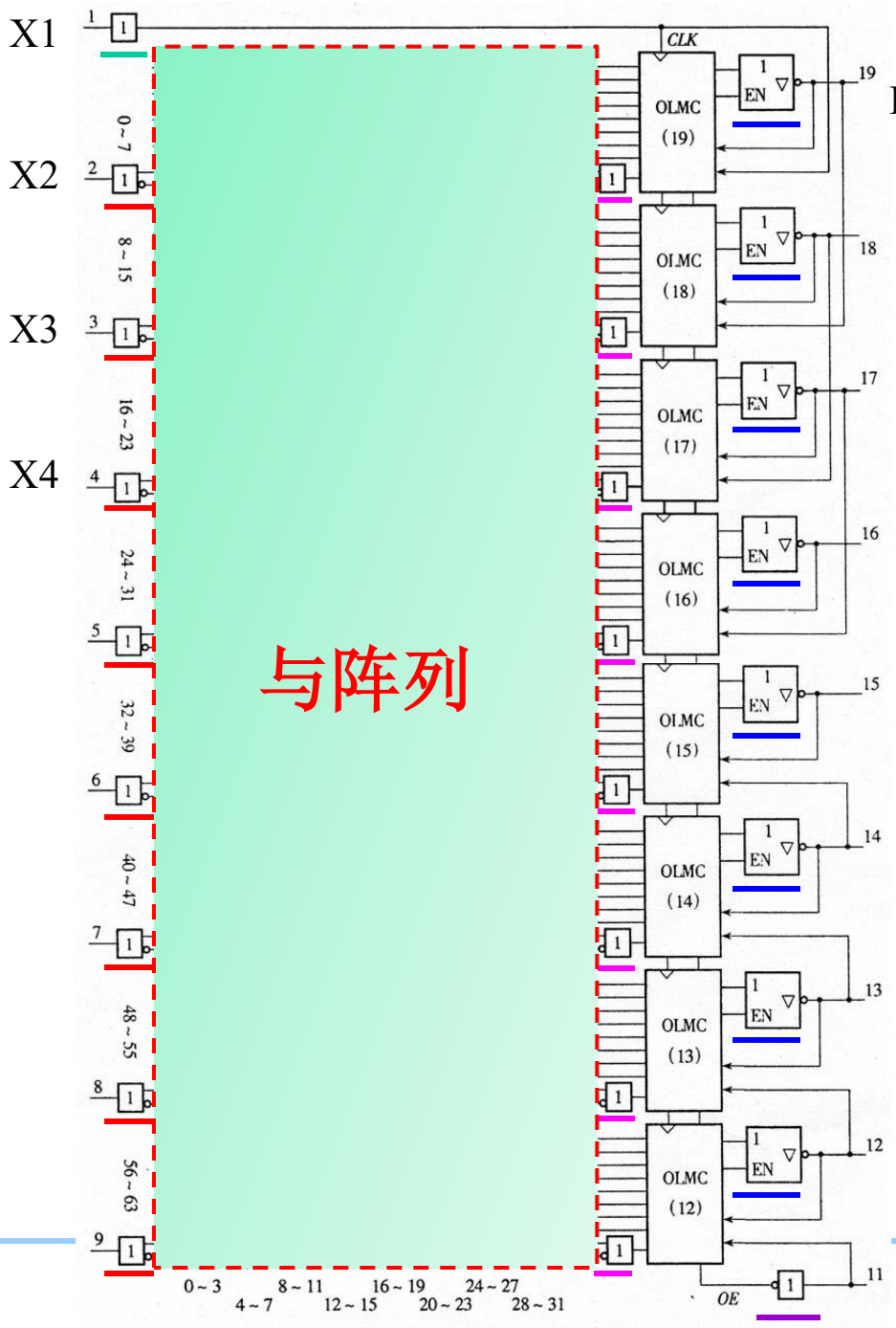


一、GAL16V8电路结构



1.最多有16个引脚作为输入端，最多有8个引脚作为输出端





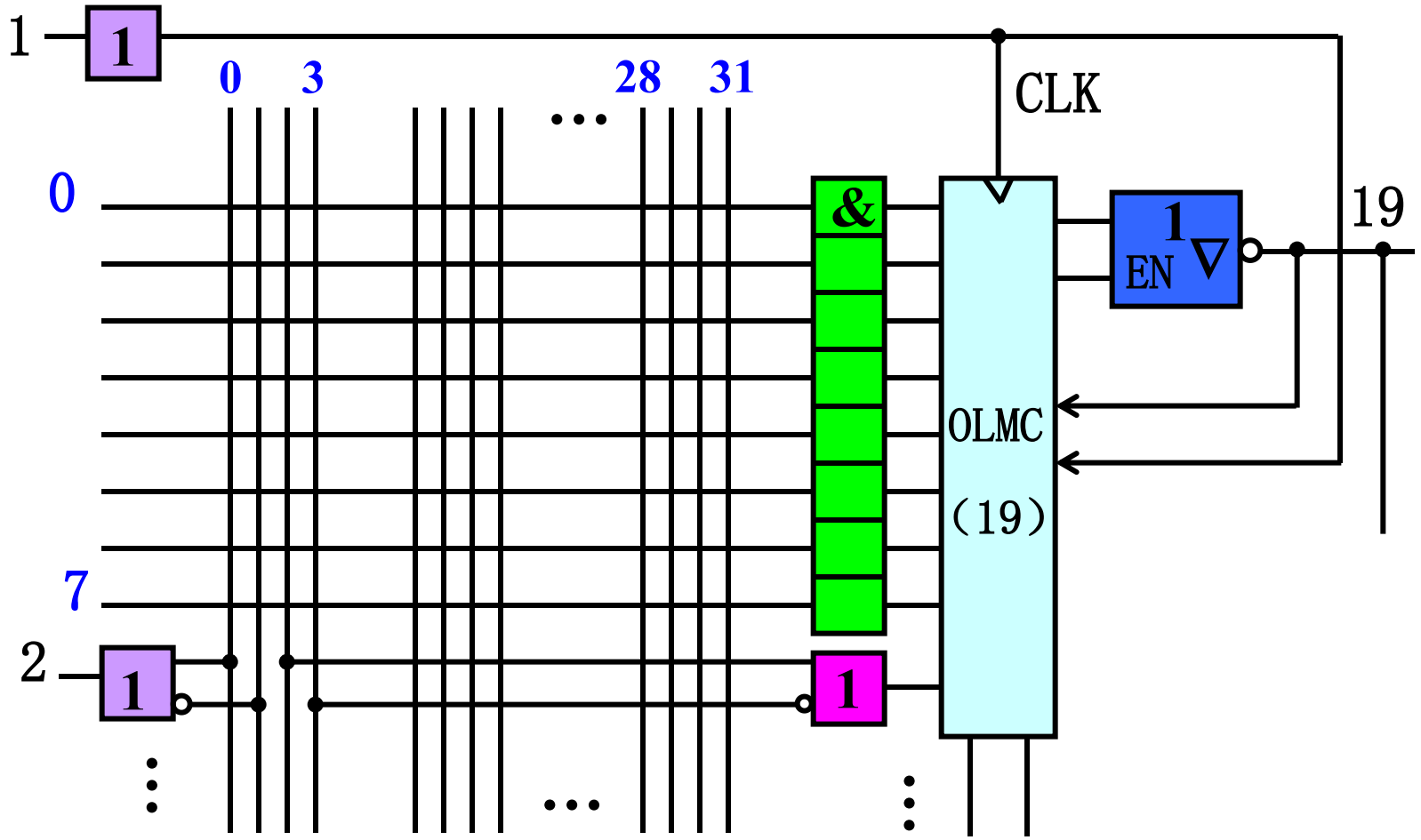
1个时钟输入缓冲器

8个输入缓冲器

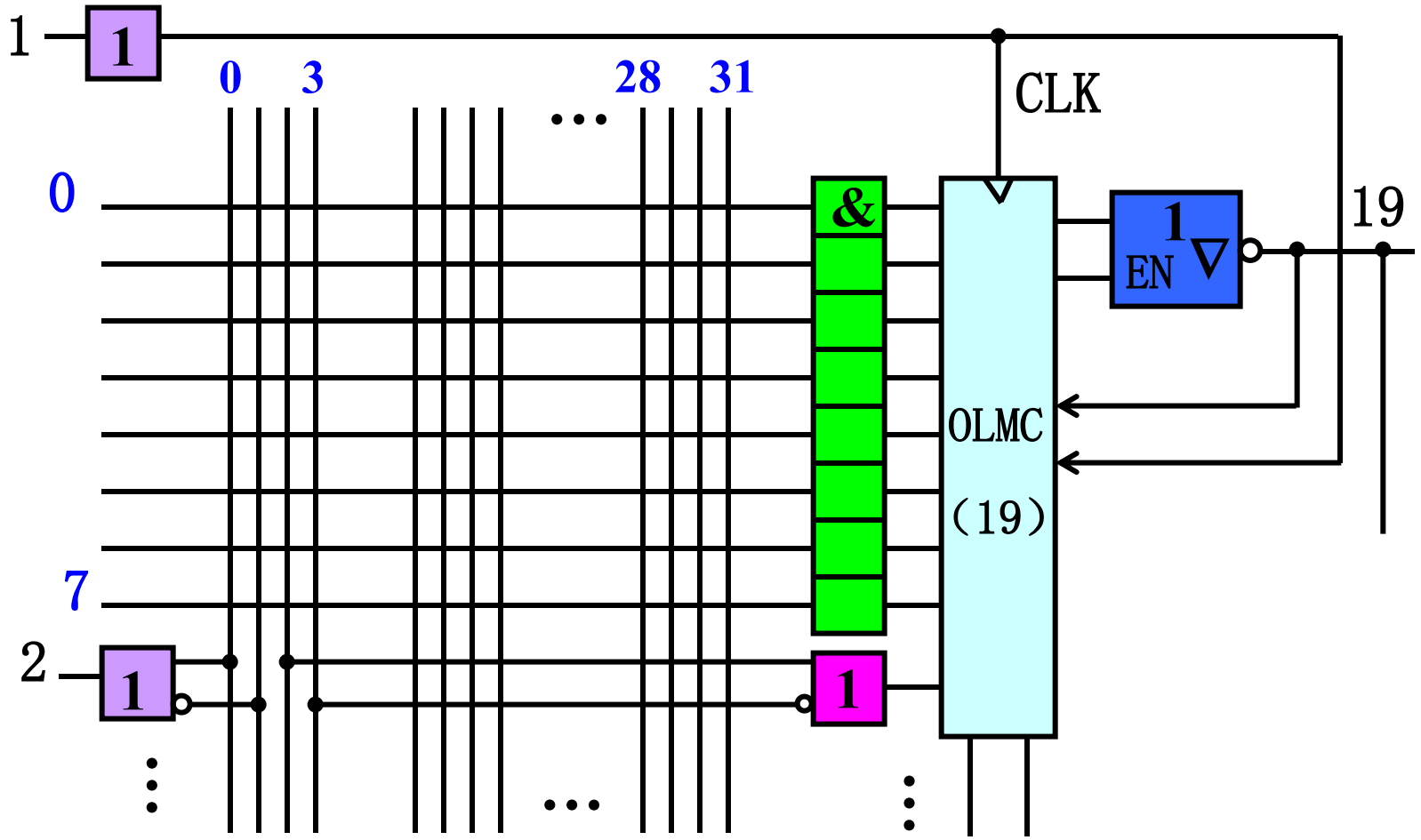
8个输出反馈缓冲器

1个选通信号输入反相器

8个输出反相器



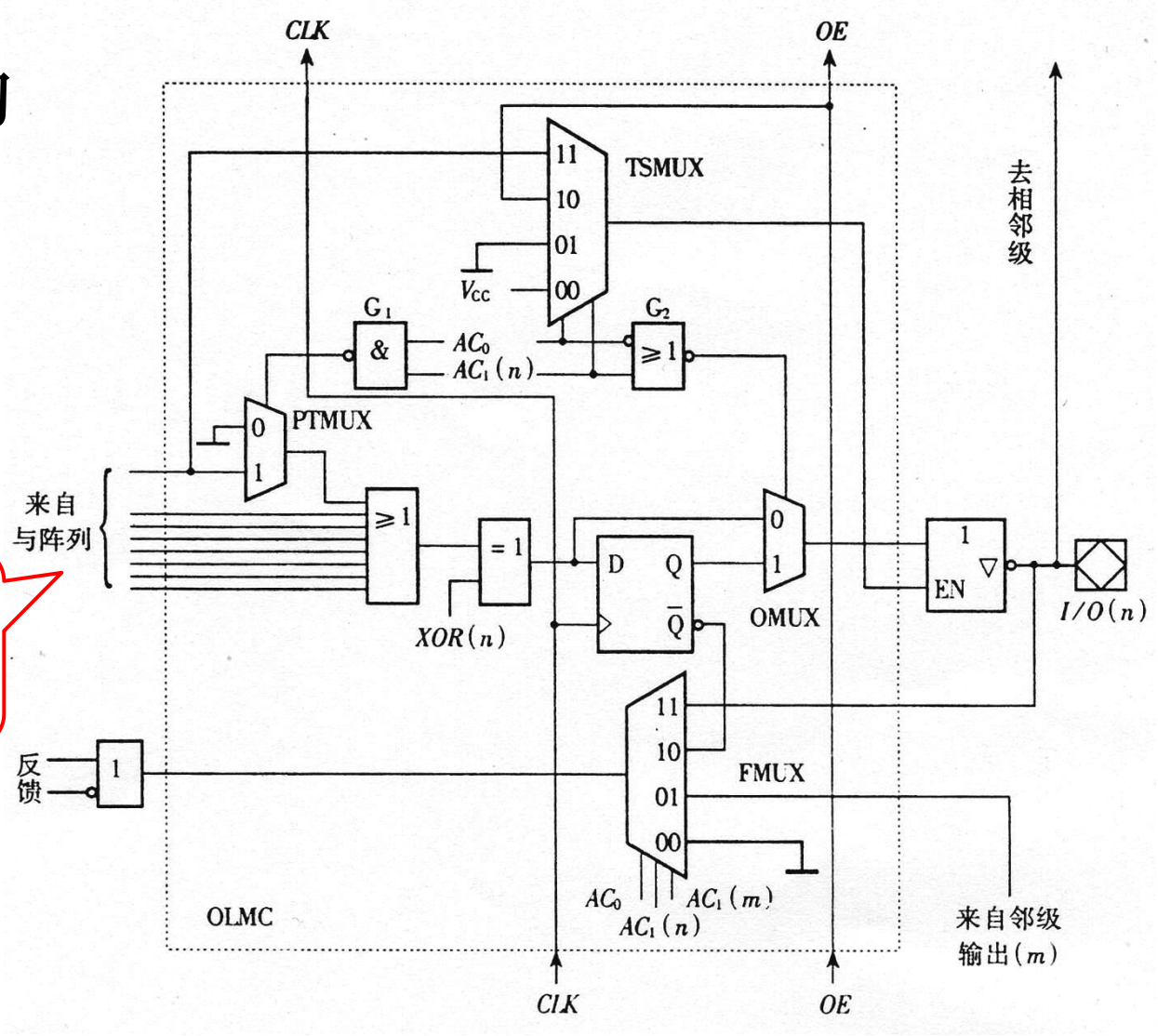
2.8×8个与门，可实现64个乘积项(Product Term)



3.每个与门可实现16个变量相乘

二、GAL16V8的OLMC*61-66

1. OLMC的结构



一个OLMC输出端最多包含8个乘积项

2. OLMC的配置

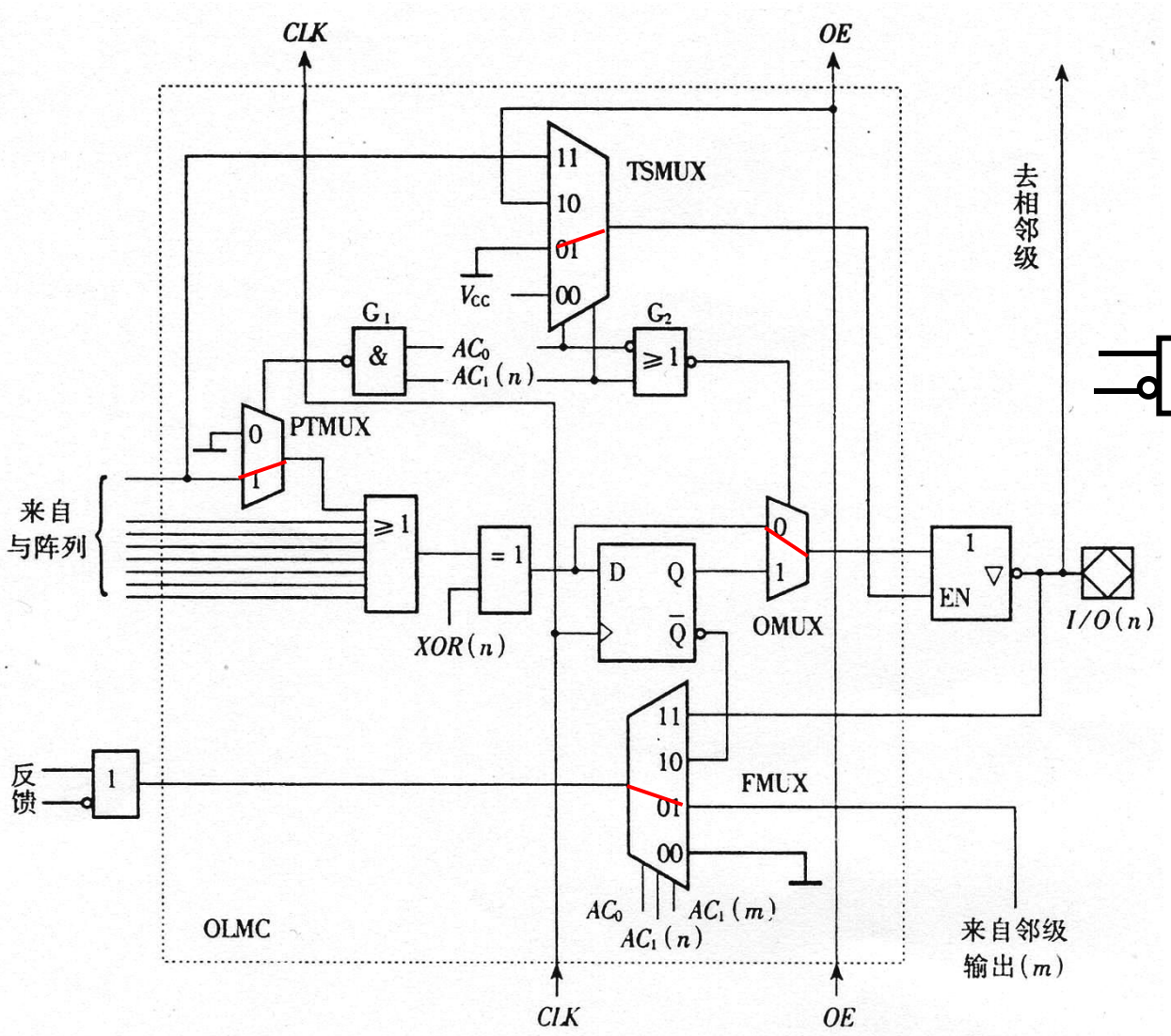
(1) SYN(Synchronous)、AC_0、AC_1(n)只能取

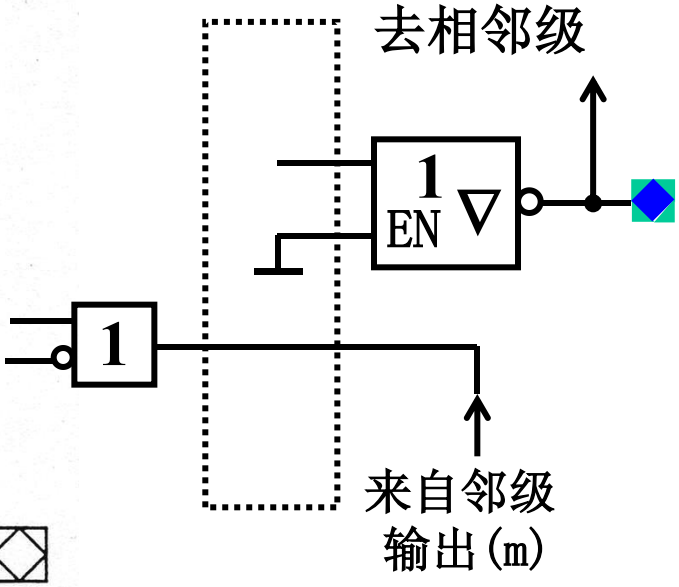
“101、100” (simple mode)

或“111” (complex mode)

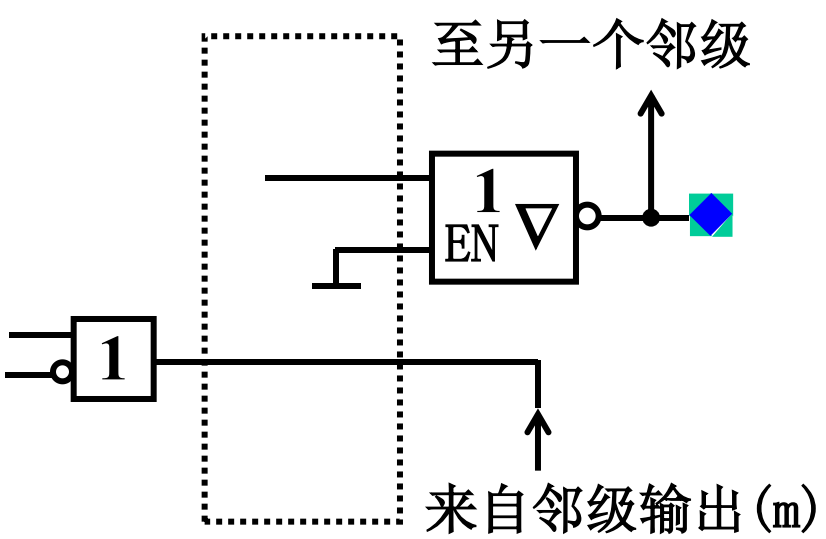
或“011、010” (registered mode)

在SYN AC_0 AC_1(n) =101时

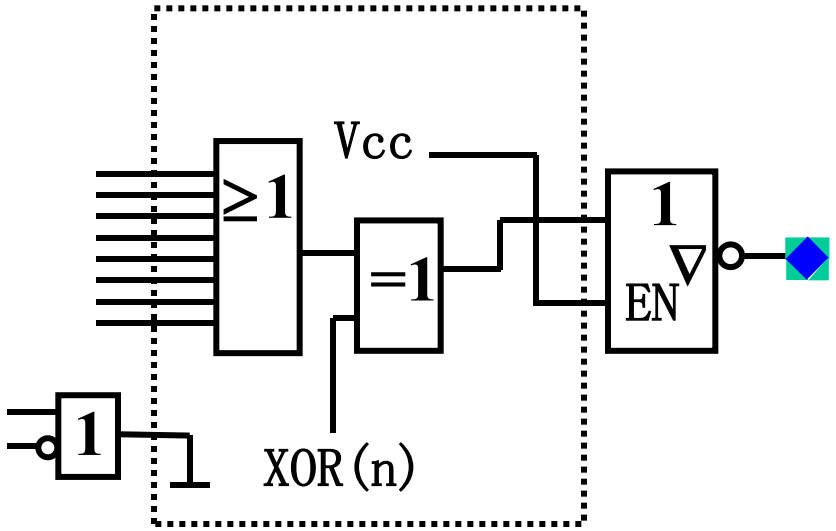




(2) 在SYN AC_0 AC_1(n) =101、100时(simple mode)

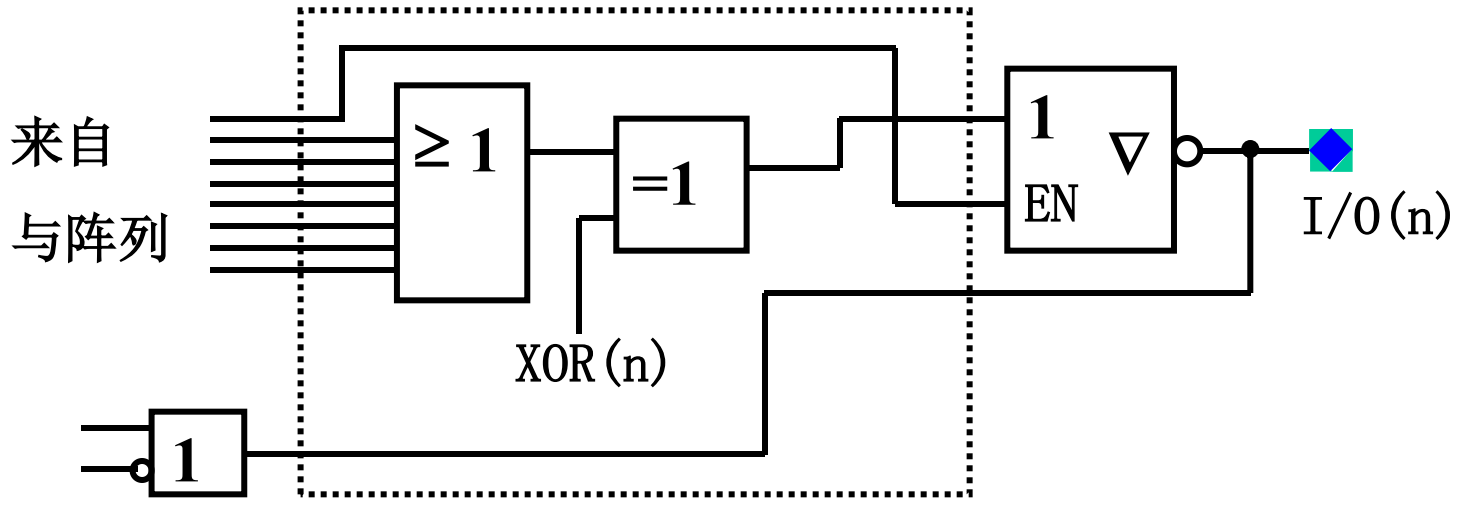


(a) 专用输入模式



(b) 专用组合输出模式

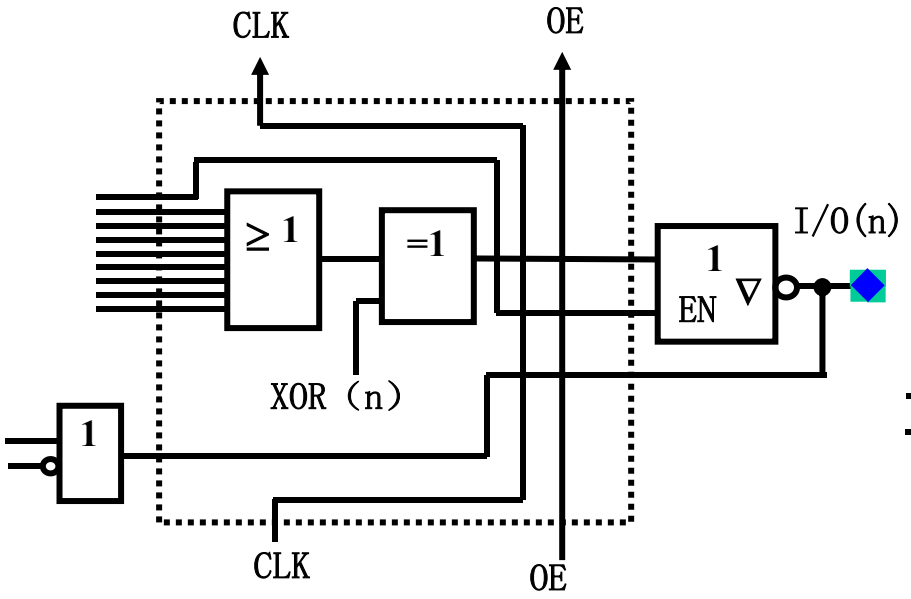
(3)在SYN AC_0 AC_1(n) = 111时（complex mode）



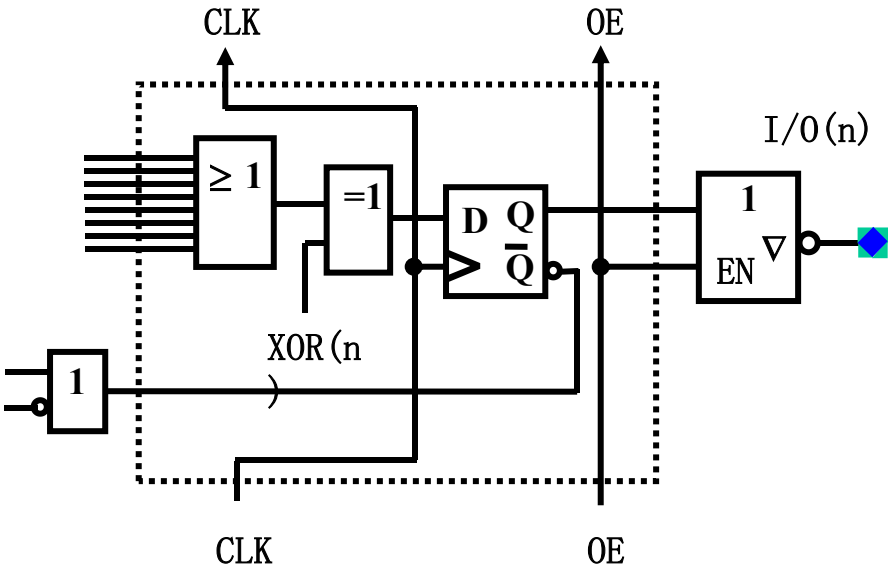
（c）反馈组合输出模式

(4)在SYN AC_0 AC_1(n) = 011、010时 (registered mode)

1、11引脚只能分别作clock、output enable端。



（d）时序电路中的组合输出模式



(e)寄存器输出模式

思考题

1.用PLD设计组合电路的原理是什么？

作业题

6.4
6.5